In the claims:

Claims 1-26 (Previously cancelled).

27. (Previously amended) An electrically programmable and erasable memory device comprising:

a substrate of semiconductor material of a first conductivity type;

first and second spaced-apart regions of a second conductivity type formed in the substrate, with a channel region therebetween;

an electrically conductive floating gate disposed over and insulated from a portion of said channel region and a portion of the first region, wherein the floating gate consists of a first portion and a second portion integrally formed together;

an electrically conductive source region disposed over and electrically connected to the first region in the substrate, the source region having a lower portion that is disposed adjacent to and insulated from the floating gate and an upper portion that is disposed over and insulated from the floating gate first portion and not the floating gate second portion; and

an electrically conductive control gate having a first portion and a second portion, the first control gate portion being disposed adjacent to and insulated from the floating gate, and the second control gate portion being disposed over and insulated from the floating gate second portion and not the floating gate first portion.

28. (Original) The device of claim 27, wherein the source region upper portion has a greater width than that of the source region lower portion.

29. (Original) The device of claim 28, wherein the source region has a substantially T-shaped cross-section.

30. (Previously amended) The device of claim 27, further comprising:

an insulation layer disposed between the floating gate and the control gate, and having a thickness permitting Fowler-Nordheim tunneling of charges therethrough.

31. (Previously amended) An array of electrically programmable and erasable memory devices comprising:

a substrate of semiconductor material of a first conductivity type;

spaced apart isolation regions formed on the substrate which are substantially parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions; and

each of the active regions including a column of pairs of memory cells extending in the first direction, each of the memory cell pairs including:

a first region and a pair of second regions spaced apart in the substrate and having a second conductivity type, with channel regions formed in the substrate between the first region and the second regions,

a pair of electrically conductive floating gates each disposed over and insulated from a portion of one of the channel regions and a portion of the first region, wherein each of the floating gates consists of a first portion and a second portion integrally formed together,

an electrically conductive source region disposed over and electrically connected to the first region in the substrate, the source region having a lower portion that is disposed adjacent to and insulated from the pair of floating gates and an upper portion that is disposed over and insulated from the floating gate first portions and not the floating gate second portions; and

a pair of electrically conductive control gates each having a first portion and a second portion, wherein for each of the control gates, the first control gate portion is disposed adjacent to and insulated from one of the floating gates and the second control gate portion is disposed over and insulated from the second portion and not the first portion of the one floating gate.

32. (Original) The device of claim 31, wherein the source region upper portion has a greater width than that of the source region lower portion.

33. (Original) The device of claim 32, wherein the source region has a substantially T-shaped cross-section.

34. (Original) The device of claim 31, wherein each of the source regions extends across the active regions and isolation regions in a second direction substantially perpendicular to the first direction and intercepts one of the memory cell pairs in each of the active regions.

35. (Previously amended) The device of claim 31, wherein each of the memory cell pairs further comprises:

an insulation layer disposed between each of the floating gates and each of the control gates and having a thickness permitting Fowler-Nordheim tunneling of charges therethrough.

36. (Original) The device of claim 35, wherein each of the control gates extends across the active regions and isolation regions in a second direction substantially perpendicular to the first direction and intercepts one of the memory cell pairs in each of the active regions.

37. (Currently amended) The device of claim 27, further comprising:

insulation material disposed between the source region [~~second~~] upper portion and the floating gate first portion, and having a thickness for permitting voltage coupling therebetween.

38. (Currently amended) The device of claim 31, wherein each of the memory cell pairs further comprises:

insulation material disposed between the source region [~~second~~] upper portion and each of the floating gate first portions, and having a thickness for permitting voltage coupling therebetween.

39. (New) An electrically programmable and erasable memory device comprising:

a substrate of semiconductor material of a first conductivity type;

first and second spaced-apart regions of a second conductivity type formed in the substrate, with a channel region therebetween;

an electrically conductive floating gate disposed over and insulated from a portion of said channel region and a portion of the first region;

an electrically conductive source region electrically connected to the first region in the substrate, the source region having a lower portion that is disposed adjacent to and insulated from the floating gate and an upper portion that is disposed over and insulated from the floating gate; and

an electrically conductive control gate having a first portion and a second portion, the first control gate portion being disposed adjacent to and insulated from the floating gate, and the second control gate portion being disposed over and insulated from the floating gate;

wherein the source region upper portion is disposed adjacent to and insulated from the second control gate portion, with no vertical overlap therebetween.

40. (New) The device of claim 39, further comprising:

insulation material disposed between the source region lower portion and the floating gate having a thickness permitting voltage coupling therethrough; and

insulation material disposed between the source region upper portion and the floating gate having a thickness permitting voltage coupling therethrough.

41. (New) The device of claim 40, further comprising:

insulation material disposed between the floating gate and the control gate having a thickness permitting Fowler-Nordheim tunneling of charges therethrough.

42. (New) An array of electrically programmable and erasable memory devices comprising:

a substrate of semiconductor material of a first conductivity type;

spaced apart isolation regions formed on the substrate which are substantially parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions; and

each of the active regions including a column of pairs of memory cells extending in the first direction, each of the memory cell pairs including:

a first region and a pair of second regions spaced apart in the substrate and having a second conductivity type, with channel regions formed in the substrate between the first region and the second regions,

a pair of electrically conductive floating gates each disposed over and insulated from a portion of one of the channel regions and a portion of the first region,

an electrically conductive source region electrically connected to the first region in the substrate, the source region having a lower portion that is disposed adjacent to and insulated from the pair of floating gates and an upper portion that is disposed over and insulated from the floating gates, and

a pair of electrically conductive control gates each having a first portion and a second portion, wherein for each of the control gates, the first control gate portion is disposed adjacent to and insulated from one of the floating gates and the second control gate portion is disposed over and insulated from the one floating gate, and wherein each of the control gate second portions is disposed adjacent to and insulated from the source region upper portion with no vertical overlap therebetween.

43. (New) The device of claim 42, wherein each of the source regions extends across the active regions and isolation regions in a second direction substantially perpendicular to the first direction and intercepts one of the memory cell pairs in each of the active regions.

44. (New) The device of claim 42, wherein each of the memory cell pairs further comprises:

insulation material disposed between the source region lower portion and the pair of floating gates having a thickness permitting voltage coupling therethrough; and

insulation material disposed between the source region upper portion and the pair of floating gates having a thickness permitting voltage coupling therethrough.

45. (New) The device of claim 44, wherein each of the memory cell pairs further comprises:

insulation material disposed between each of the floating gates and one of the control gates and having a thickness permitting Fowler-Nordheim tunneling of charges therethrough.